1. A method of fabricating a silicon mirror device comprising:

providing a p-doped single crystal silicon substrate wafer having a frontside and a backside;

forming first and second n-doped regions at a surface of said substrate wherein said first n-doped regions have a first thickness and said second n-doped regions have a second thickness larger than said first thickness;

forming a hard mask on said backside of said wafer;

depositing a silicon oxide layer on said frontside of said wafer;

depositing an aluminum layer on said silicon oxide layer and patterning said aluminum layer to leave aluminum on said silicon oxide layer overlying some of said second n-doped regions to form thermal actuators;

depositing a dielectric layer overlying said patterned aluminum layer and said silicon oxide layer and patterning said dielectric layer to form a mask for flexible springs over portions of said first n-doped regions;

depositing and patterning a metal layer overlying said dielectric layer to form bond pads to said thermal actuators contacting said patterned aluminum layer through openings in said dielectric layer and to form reflecting mirror surfaces overlying others of said second n-doped regions not covered by said patterned aluminum layer to form micromirrors;

thereafter etching away said substrate from said backside of said wafer stopping at said first and second n-doped regions;

thereafter dicing said wafer into mirror array chips;

thereafter etching away said dielectric layer from said frontside of said wafer to expose portions of said first n-doped regions; and

etching away from said frontside said exposed first n-doped regions not covered by said mask to form flexible springs in said first n-doped regions wherein said second n-doped regions covered by said patterned aluminum layer form thermal actuators and said wherein said flexible springs connect said micromirrors to said thermal actuators.

2. The method according to Claim 1 wherein said forming said first and second n-doped regions comprises:

implanting first phosphorus ions through a mask into said substrate to a first depth; and

implanting second phosphorus ions globally into said substrate to a second depth shallower than said first depth wherein said first depth is increased to a third depth wherein said phosphorus ions diffused to said second depth form said first n-doped regions and wherein said phosphorus ions diffused to said third depth form said second n-doped regions.

3. The method according to Claim 1 wherein said forming said first and second n-doped regions comprises:

growing an epitaxial silicon layer on said p-doped silicon substrate; and

patterning said epitaxial silicon layer to form said first n-doped regions and said second n-doped regions.

4. The method according to Claim 3 wherein said patterning is performed using a deep reactive ion etching (DRIE) process.

5. The method according to Claim 1 wherein said forming said hard mask comprises:

depositing a first nitride layer on said substrate on said backside of said wafer;

depositing a TEOS oxide layer overlying said first nitride layer; and

depositing a second nitride layer overlying said TEOS oxide layer to form said hard mask.

6. The method according to Claim 5 wherein said first nitride layer is deposited to a thickness of between about 1200 and 1800 Angstroms, said TEOS oxide layer is deposited by plasma enhanced chemical vapor deposition (PECVD) to a thickness of between about 800 and 1200 Angstroms, and said second nitride layer is deposited by PECVD to a thickness of between about 1500 and 2500 Angstroms.

7. The method according to Claim 1 wherein said aluminum layer is deposited to a thickness of about 1 micron.

8. The method according to Claim 1 wherein said depositing said metal layer comprises:

depositing a chromium layer to a thickness of between about 100 and 200 Angstroms; and

depositing a gold layer overlying said chromium layer to a thickness of between about 400 and 600 Angstroms.

9. The method according to Claim 1 wherein said etching away said substrate from said backside of said wafer comprises electrochemical etching in aqueous KOH.

10. The method according to Claim 1 wherein said etching away said substrate from said backside of said wafer comprises a combination of DRIE and electrochemical etching in aqueous KOH.

11. The method according to Claim 1 wherein said etching away said dielectric layer from said top side of said wafer comprises DRIE.

12. The method according to Claim 1 wherein said etching away said dielectric layer from said top side of said wafer separates said thermal actuators, said flexible springs, and said micromirrors simultaneously.

13. The method according to Claim 1 wherein edges of said micromirrors are thinner than central portions of said micromirrors.

14. A method of fabricating a silicon mirror device comprising:

providing a p-doped single crystal silicon substrate wafer having a frontside and a backside;

forming first and second n-doped regions at a surface of said substrate wherein said first n-doped regions have a first thickness and said second n-doped regions have a second thickness larger than said first thickness;

forming a hard mask on said backside of said wafer;

depositing a silicon oxide layer on said frontside of said wafer;

depositing an aluminum layer on said silicon oxide layer and patterning said aluminum layer to leave aluminum on said silicon oxide layer overlying some of said second n-doped regions to form thermal actuators;

depositing a dielectric layer overlying said patterned aluminum layer and said silicon oxide layer and patterning said dielectric layer to form a mask for flexible springs over portions of said first n-doped regions;

depositing and patterning a metal layer overlying said dielectric layer to form bond pads to said thermal actuators contacting said patterned aluminum layer through openings in said dielectric layer and to form reflecting mirror surfaces overlying others of said second n-doped regions not covered by said patterned aluminum layer to form micromirrors;

thereafter etching away said substrate from said backside of said wafer stopping at said first and second n-doped regions;

thereafter dicing said wafer into mirror array chips;

thereafter etching away said dielectric layer from said frontside of said wafer to expose portions of said first n-doped regions; and

etching away from said frontside said exposed first n-doped regions not covered by said oxide mask to form flexible springs in said first n-doped regions wherein said second n-doped regions covered by said patterned aluminum layer form thermal actuators and wherein said flexible springs connect said micromirrors to said thermal actuators and wherein each mirror element in each of said mirror array chips comprises one micromirror and four thermal actuators.

15. The method according to Claim 14 wherein said forming said first and second n-doped regions comprises:

implanting first phosphorus ions through a mask into said substrate to a first depth; and

implanting second phosphorus ions globally into said substrate to a second depth shallower than said first depth wherein said first depth is increased to a third depth wherein said phosphorus ions diffused to said second depth form said first n-doped regions and wherein said phosphorus ions diffused to said third depth form said second n-doped regions.

16. The method according to Claim 14 wherein said forming said first and second n-doped regions comprises:

growing an epitaxial silicon layer on said p-doped silicon substrate; and

patterning said epitaxial silicon layer to form said first n-doped regions and said second n-doped regions.

17. The method according to Claim 16 wherein said patterning is performed using a deep reactive ion etching (DRIE) process.

18. The method according to Claim 14 wherein said forming said hard mask comprises:

depositing a first nitride layer on said substrate on said backside of said wafer;

depositing a TEOS oxide layer overlying said first nitride layer; and

depositing a second nitride layer overlying said TEOS oxide layer to form said hard mask.

19. The method according to Claim 18 wherein said first nitride layer is deposited to a thickness of between about 1200 and 1800 Angstroms, said TEOS oxide layer is deposited by plasma enhanced chemical vapor deposition (PECVD) to a thickness of between about 800 and 1200 Angstroms, and

said second nitride layer is deposited by PECVD to a thickness of between about 1500 and 2500 Angstroms.

20. The method according to Claim 14 wherein said aluminum layer is deposited to a thickness of about 1 micron.

21. The method according to Claim 14 wherein said depositing said metal layer comprises:

depositing a chromium layer to a thickness of between about 100 and 200 Angstroms; and

depositing a gold layer overlying said chromium layer to a thickness of between about 400 and 600 Angstroms.

22. The method according to Claim 14 wherein said etching away said substrate from said backside of said wafer comprises electrochemical etching in aqueous KOH.

23. The method according to Claim 14 wherein said etching away said substrate from said backside of said wafer comprises a combination of DRIE and electrochemical etching in aqueous KOH.

24. The method according to Claim 14 wherein said etching away said dielectric layer from said top side of said wafer comprises DRIE.

25. The method according to Claim 14 wherein said etching away said dielectric layer from said top side of said wafer separates said thermal actuators, said flexible springs, and said micromirrors simultaneously.

26. The method according to Claim 14 wherein edges of said micromirrors are thinner than central portions of said micromirrors.

27. A three-dimensional free space micromirror device comprising:

single crystal silicon micromirrors;

single crystal silicon thermal actuators; and

single crystal silicon flexible springs connecting said thermal actuators to said micromirrors.

28. The device according to Claim 27 wherein each said micromirror comprises a reflecting surface on said single crystal silicon and a dielectric layer therebetween.

29. The device according to Claim 28 wherein said reflecting surface comprises a layer of chromium having a thickness of between about 100 and 200 Angstroms and an overlying layer of gold having a thickness of between about 400 and 600 Angstroms.

30. The device according to Claim 27 wherein said thermal actuators comprise an aluminum film overlying said single crystal silicon and having a silicon dioxide layer therebetween for electrical isolation.

31. The device according to Claim 27 wherein said single crystal silicon forming said micromirrors, said thermal actuators, and said flexible springs is n-doped.

32. The device according to Claim 27 further comprising bond pads connected to said thermal actuators wherein said thermal actuators are attached to fixed supports on a substrate through said bond pads.

33. The device according to Claim 27 wherein each mirror element of said micromirror device comprises one micromirror joined with four of said thermal actuators through four of said flexible springs at four corners symmetrically and wherein each of said thermal actuators are attached to fixed supports on a substrate.

34. The device according to Claim 27 wherein said micromirror has a diameter of between about 200 and 600 microns and a silicon thickness of about 10 microns and wherein edges of said micromirror are thinner than a central portion of said micromirror.

35. The device according to Claim 30 wherein said thermal actuators have a length of between about 300 and 500 microns, a silicon thickness of about 2 microns, a silicon dioxide thickness of 0.2 microns, and an aluminum thickness of about 1 micron.

36. The device according to Claim 34 wherein said flexible springs have a thickness of about 2 microns.

37. The device according to Claim 27 wherein said thermal actuators allow said device to achieve a deflection angle of up to about 10 degrees.